

Yibo Hou

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EDUCATION

University of Illinois Urbana-Champaign (UIUC)

B.S. in Electrical & Computer Engineering with Minor in Computer Science

Urbana, IL

2024–2028

GPA: 3.94/4.00 | ECE Scholarship | Grainger Engineering Achievement Scholarship | Justin David Cunningham Memorial Award

Honors & Memberships: Dean's List (Fall 2024, Fall 2025, Spring 2026) | James Scholar Honors | Eta Kappa Nu (HKN)

SELECTED HARDWARE PROJECTS

FPGA Limit Order Book | SystemVerilog, Artix-7, Questa UVM, Python

Mar 2026–Aug 2026

- Architected a price-time-priority engine with an 8,191-order BRAM pool and 4-way hash table; measured a 9-cycle (72 ns) core first-trade path on a 125 MHz diagnostic FPGA image.
- Implemented Fast and Drain FSM paths with a crossing-ADD register bypass and parallel bid/ask reads; estimated peak core throughput of 9.6M commands/s at 125 MHz.
- Integrated a shared 32-byte protocol across 1 Gbps UDP/RGMII, synthesizable RTL, and a bit-exact Python model for ADD, CANCEL, MODIFY, and EXECUTE operations.
- Built a Questa UVM scoreboard for matching sweeps and boundary cases; passed a paced 1,000-command board stress test with 100% ACK success and closed post-route timing at 125 MHz.

Artix-7 FPGA Graphics Engine | SystemVerilog, Vivado/Vitis, MicroBlaze

Sep 2025–Jan 2026

- Architected a 720p60 graphics subsystem from MicroBlaze game control and a handwritten tile/sprite renderer through AXI4-Stream/VDMA into a 512 MiB DDR3 triple-frame-buffer path and custom TMDS/HDMI output.
- Allocated three 2 MiB-aligned RGB565 frame buffers with frame-boundary switching to decouple rendering from scanout and prevent tearing across the 100 MHz MIG AXI and 74.25 MHz pixel domains.
- Designed a stall-safe renderer for a 128×64 tile map and 16 32×32 sprites, producing one RGB565 pixel per accepted clock with ready/valid backpressure and BRAM-backed indexed-color assets.
- Integrated FAT32 SD-card assets, UART input, AXI VDMA, an asynchronous pixel FIFO, and an OSERDESE2-based TMDS transmitter; completed implementation and timing closure at +0.848 ns WNS.

AD/DA UDP Oscilloscope & Waveform Generator | SystemVerilog, Artix-7, Ethernet

May 2026–Aug 2026

- Built a processor-free 25 MSPS ADC-to-UDP pipeline and host-controlled DAC return path around custom RTL UDP/IP/RGMII, dynamic ARP, and Gray-code asynchronous FIFOs across 25/125 MHz clock domains.
- Packetized 736 ADC samples into 1,472-byte UDP payloads, buffered 4,096 DAC samples in BRAM, and developed an interface for live display, telemetry, and waveform upload.
- Sustained approximately 34,200 UDP packets/s with zero loss across roughly 45 billion samples, automatic link recovery, and +0.145 ns post-route WNS.

RISC-V ASIC & Custom VLSI Flow | Cadence Virtuoso/Innovus, SystemVerilog

Jan 2026–May 2026

- Designed 13 transistor-level CMOS standard cells in FreePDK45, completed DRC/LVS, and generated LEF/Liberty views for synthesis and physical design.
- Manually laid out and verified a 32-bit bit-sliced RISC-V datapath, including the ALU, comparator, barrel shifter, and register-file macros, using reusable transistor-level standard cells.
- Completed full-chip Innovus PnR using the custom library, 32 register-file hard macros, power rings/strips, and a six-metal signal-routing stack.

Custom Folded-Cascode LDO Regulator | Cadence Virtuoso, Spectre, g_m/I_D sizing

Jan 2026–May 2026

- Designed a transistor-level 1.2 V LDO with a PMOS-input folded-cascode error amplifier, resistive feedback, compensation network, and g_m/I_D -based device sizing.
- Achieved 83.1 dB loop gain, 75.2°–84.4° phase margin, and 1.27–1.29 MHz unity-gain frequency across evaluated load points.
- Verified 6 $\mu\text{V}/\text{mA}$ load regulation and characterized line regulation and PSR from 1 kHz to 1 MHz across load conditions.

EXPERIENCE & RESEARCH

Tianyi Transportation Technology, China Telecom | Systems Engineering Intern | Suzhou, China

May 2025–Aug 2025

- Developed ROS 2 radar stress-test and monitoring tools with real-time frame-loss diagnostics, reducing manual logging time by 60%.
- Migrated a millimeter-wave radar driver from UDP to CAN for deterministic integration; validated multiple LiDAR systems and cross-sensor timing with IEEE 802.1AS PTP, NTP, and GPS synchronization.
- Deployed offline Docker images from IPv6 registries to support containerized radar and LiDAR perception pipelines.

Cunjiang Yu Research Group, UIUC | Research Assistant (15 hrs./week) | Urbana, IL

Feb 2025–Present

- Designed silicon microelectrode arrays and microparticles for retinal prosthesis, cardiac pacing, and neural-stimulation research.
- Fabricated and characterized 200 μm NIP semiconductor electrodes to evaluate retinal-prosthesis performance.

COURSEWORK

Computer Organization & Design (Ongoing), Digital IC Design (Ongoing), Analog IC Design, VLSI System Design, Digital Systems Laboratory, Semiconductor Devices, Digital Signal Processing, Data Structures

TECHNICAL SKILLS

HDL & Verification: SystemVerilog, Verilog, UVM, Questa, VCS/Verdi

FPGA & Digital Design: Vivado/Vitis, AXI4/AXI4-Stream, CDC, BRAM, DDR3, asynchronous FIFOs

IC Tools & Programming: Cadence Virtuoso/Innovus/Spectre, Ethernet/RGMII/UDP, Python, Tcl, C/C++