

OVERALL DESIGN APPROACH & SYSTEM-LEVEL TRADE-OFFS

Feedback Network & Biasing

Our goal was to regulate a 1.8 V input to a 1.2 V output. We set the reference voltage (V_{REF}) to 0.6 V and chose large feedback resistors ($R_1 = 100\text{ k}\Omega$, $R_2 = 200\text{ k}\Omega$). These values were specifically selected to minimize static power and keep the overall quiescent current as low as possible.

Amplifier Architecture Iterations

Achieving sufficient open-loop gain (A_v) to meet the strict line ($\leq 500\mu\text{V/V}$) and load ($\leq 50\mu\text{V/mA}$) regulation specifications drove our architecture choices.

- **Attempt 1 (5-Transistor OTA):** We initially used a standard 5-transistor OTA, but its low intrinsic output resistance (r_{ds}) yielded insufficient gain. Increasing transistor lengths to $20\mu\text{m}$ met the gain requirements but introduced massive parasitic capacitances that ruined the phase margin.
- **Attempt 2 (Folded Cascode):** We pivoted to a PMOS-input folded cascode to achieve high gain without relying on excessive channel lengths. To avoid manual trial-and-error, we used a custom Python script based on the g_m/I_D methodology to systematically size the transistors from technology data.

Frequency Compensation & The Light-Load Trade-off

We added a compensation capacitor to make the folded cascode's output the dominant pole. However, at the minimum load current of 0.1 mA, the pass transistor's output resistance (R_{out}) surged. This pushed the non-dominant output pole to a much lower frequency, moving it dangerously close to the dominant pole and failing the $\geq 45^\circ$ phase margin requirement.

To resolve this, we made a crucial system-level trade-off: we permanently added a 10 k Ω parallel dummy resistor at the output. This caps the maximum R_{out} at light loads, guaranteeing transient stability across the entire load range at the expense of drawing a higher continuous quiescent current.

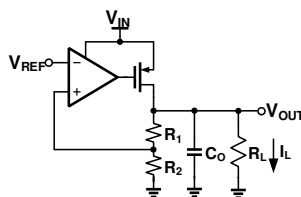


Figure 1: LDO schematic.

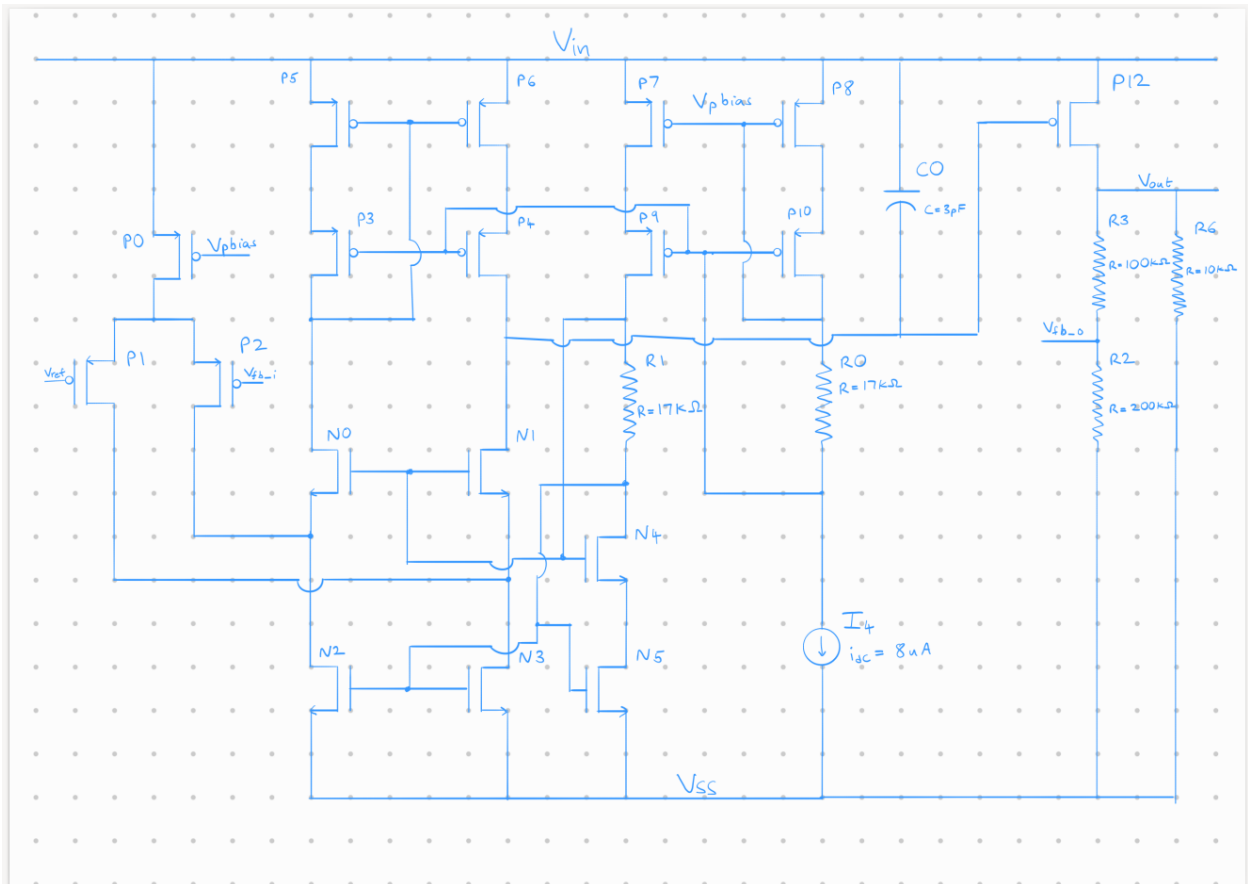


Figure 2: Schematic Diagram of Circuit

TABULATED PARAMETERS

Table 1: Tabulated MOSFET Sizes, g_m , and V_{ov}

MOSFET	Width (μm)	Height (nm)	W/L ($\mu\text{m}/\mu\text{m}$)	I_D (μA)	g_m ($\mu\text{A}/\text{V}$)	V_{ov} (mV)
P0	70.02	180	389	-58.73	1178	-30.2
P1	38.02	180	211.2222	-29.37	589.5	-19.32
P2	38.02	180	211.2222	-29.37	589.4	-19.31
P3	12.015	180	66.75	-3.846	84.1	11.9
P4	12.015	180	66.75	-3.844	84.07	11.55
P5	12.015	180	66.75	-3.846	84.05	9.678
P6	12.015	180	66.75	-3.844	84	9.689
P7	12.015	180	66.75	-8.138	166.8	-25.98
P8	12.015	180	66.75	-8	163.9	-25.69
P9	12.015	180	66.75	-8.138	165.9	-14.1
P10	12.015	180	66.75	-8	165	-21.41
P12	40000	180	222222.2222	-10120	223200	27.53
N0	9.495	540	17.5833	3.848	85.76	8.628
N1	9.495	540	17.5833	3.844	85.66	8.51
N2	37.98	540	70.3333	33.21	679.9	48.06
N3	37.98	540	70.3333	33.21	680	48.07
N4	9.495	540	17.5833	8.138	167.7	46.11
N5	9.495	540	17.5833	8.138	166.2	47.79

PERFORMANCE SUMMARY

Table 2: Performance summary

Design parameter/variable	Simulated performance	Specification
Input voltage	1.8V Nominal Voltage with a 1.62V to 1.98V Acceptable Range (i.e $\pm 10\%$ swing)	≤ 1.8 V
Output voltage	1.2 V	1.0 V – 1.4 V
Load current	10 mA	1 mA – 25 mA
DC load regulation	6 $\mu\text{V}/\text{mA}$	≤ 50 $\mu\text{V}/\text{mA}$
DC line regulation ($I_L = 0.1$ mA / $I_L = 25$ mA)	479 $\mu\text{V}/\text{V}$ / 128 $\mu\text{V}/\text{V}$	≤ 500 $\mu\text{V}/\text{V}$
Quiescent current ($I_L = 1$ mA / $I_L = 25$ mA)	0.207 mA / 0.210 mA	Minimum
PSR for $I_L = 1$ mA (@ $F_{in} = 1$ kHz / $F_{in} = 1$ MHz)	779 $\mu\text{V}/\text{V}$ / 619 mV/V	–
Worst-case PSR	832 $\mu\text{V}/\text{V}$ occurs at $I_L = 0.1$ mA	–
DC loop gain ($I_L = 1$ mA / $I_L = 25$ mA)	83.11 dB / 83.17 dB	–
Loop-gain unity gain frequency ($I_L = 1$ mA / $I_L = 25$ mA)	1.29 MHz / 1.27 MHz	–
Loop-gain phase margin ($I_L = 1$ mA / $I_L = 25$ mA)	75.22° / 84.39°	–
Loop-gain gain margin ($I_L = 1$ mA / $I_L = 25$ mA)	22.62 dB / 34.02 dB	–
Output noise ($I_L = 1$ mA / $I_L = 25$ mA)	(Optional so not included)	–

LOOP-GAIN AC RESPONSE

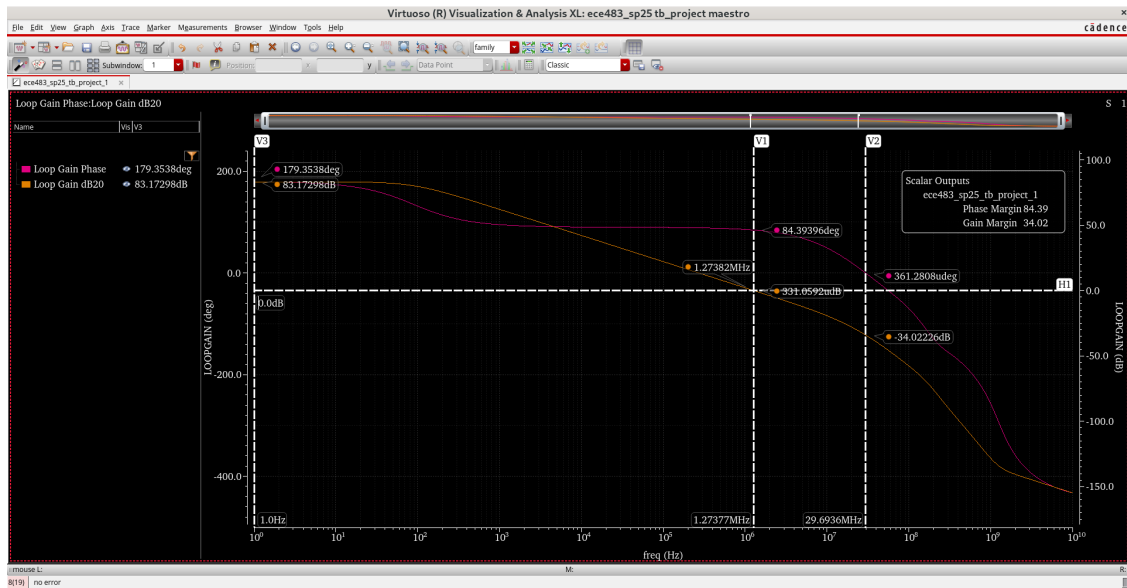


Figure 3: Loop-gain AC response for minimum current

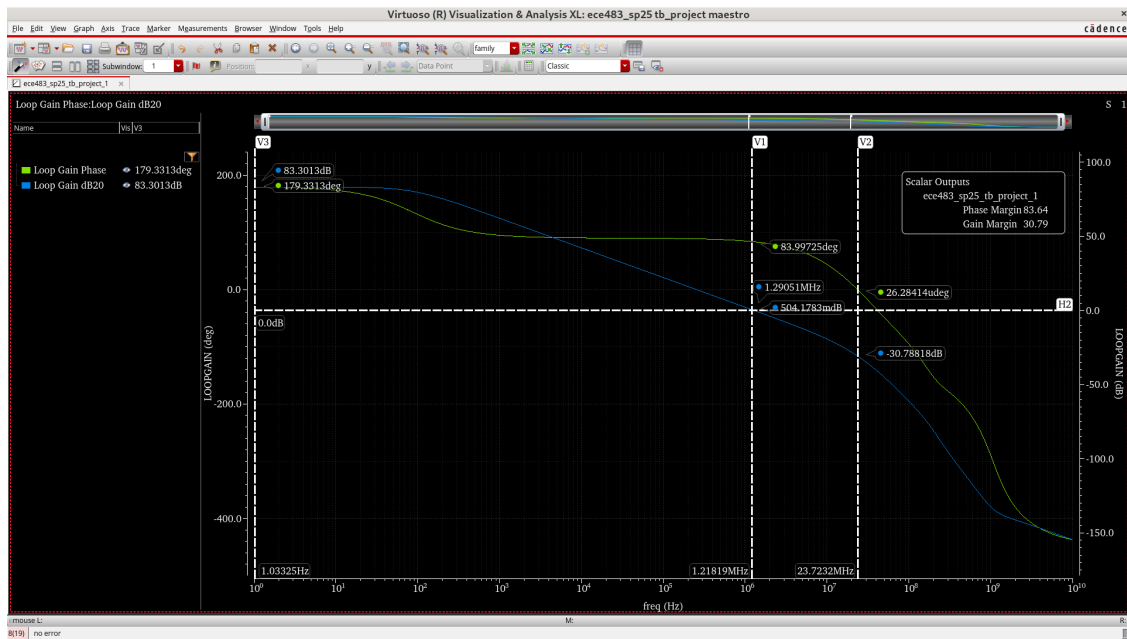


Figure 4: Loop-gain AC response for maximum current

DC LOAD AND LINE REGULATION RESPONSE

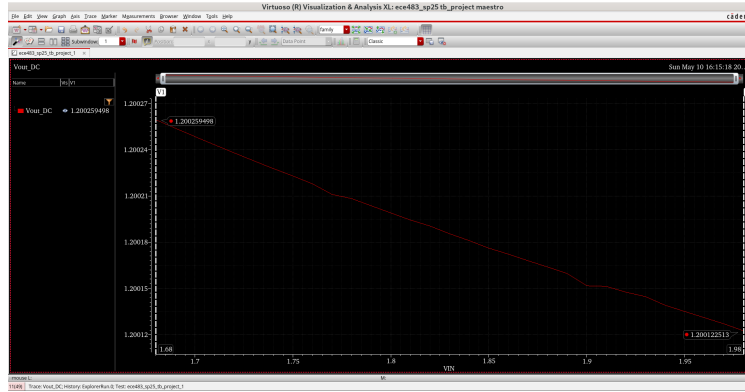


Figure 5: DC Line Regulation At Minimum Current

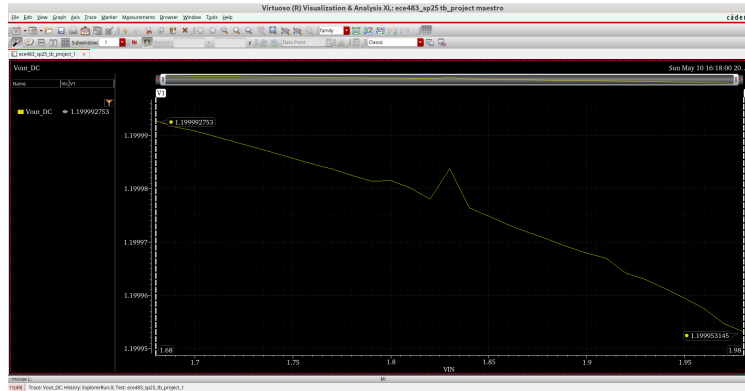


Figure 6: DC Line Regulation At Minimum Current

The formula for computing the DC line regulation is given by

$$\text{DC Line Regulation} = \frac{V_{\text{out}}(V_{\text{in,min}}) - V_{\text{out}}(V_{\text{in,max}})}{V_{\text{in,max}} - V_{\text{in,min}}}$$

Thus by using the annotate Line Regulation Parameters in the plots above, we can compute the DC Line Regulation

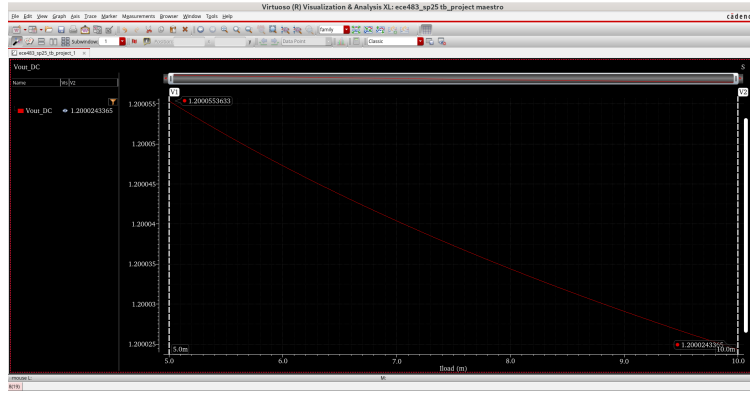


Figure 7: DC Load Regulation

The formula for computing the DC load regulation is given by

$$\text{DC Load Regulation} = \frac{V_{\text{out}}(I_{\text{load,min}}) - V_{\text{out}}(I_{\text{load,max}})}{I_{\text{load,max}} - I_{\text{load,min}}}$$

Thus by using the annotated Line Regulation Parameters in the plots above, we can compute the DC Line Regulation

POWER SUPPLY REJECTION

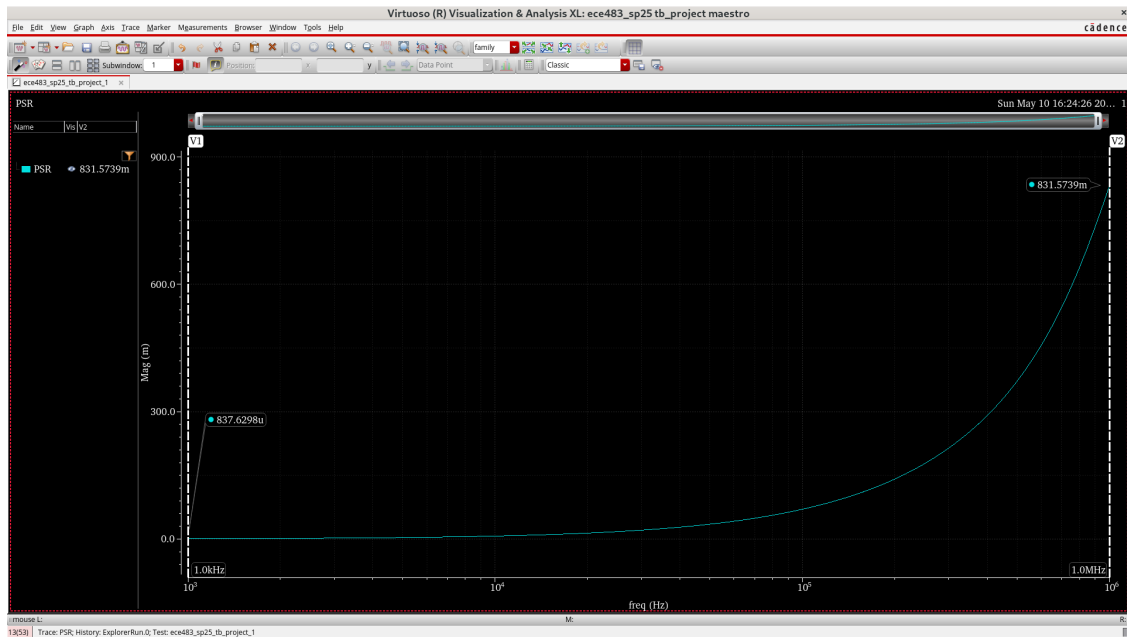


Figure 8: PSR for 1KHz to 1MHz At 0.1mA Load Current

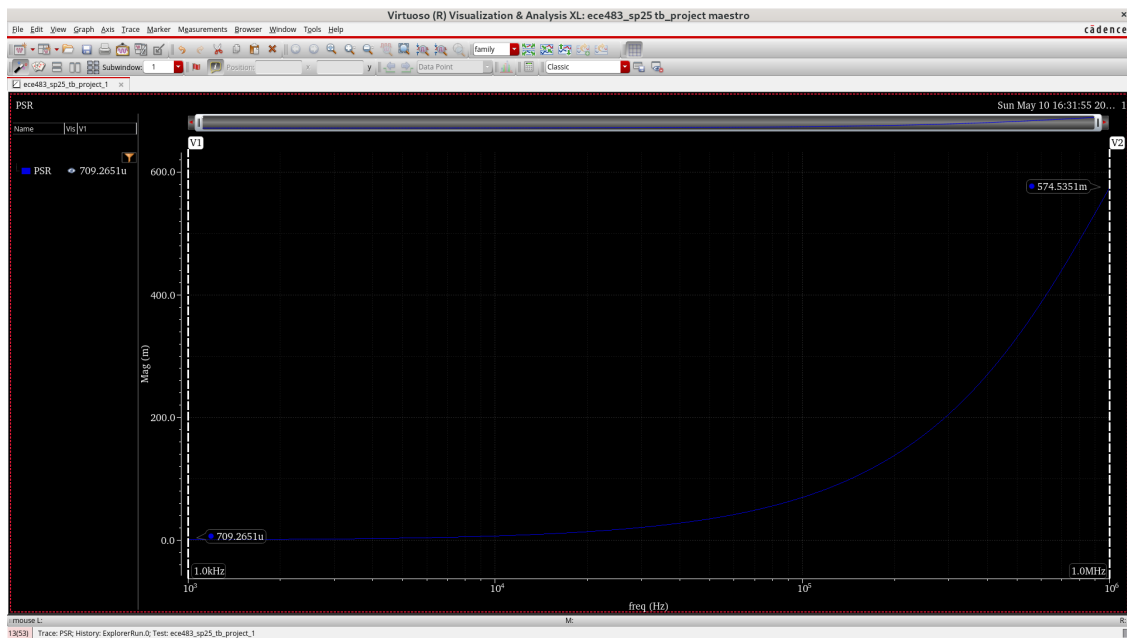


Figure 9: PSR for 1KHz to 1MHz At 25mA Load Current